

1 What is claimed is:

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3 1. A MOSFET for receiving an applied voltage and a gate  
4 voltage, the MOSFET comprising,  
5 a first terminal in a semiconductor material,  
6 a gate terminal receiving the gate voltage, the gate being  
7 disposed over a channel of the semiconductor material, the gate  
8 and channel being curved defined by a gate curvature, the gate  
9 being insulated from the semiconductor material, the channel  
10 having two channel ends, the two channel ends being nonparallel  
11 nonaligned channel ends, the curve of the gate and the channel  
12 are noninflecting,

13 an insulator disposed between the gate and the semiconductor  
14 material, and

15 a second terminal in the semiconductor material, the applied  
16 voltage extends between the first terminal and the second  
17 terminal, the gate voltage serving to control conduction  
18 between the first terminal and the second terminal in the  
19 presence of the gate voltage, the applied voltage serving to  
20 establish a diverging electric field extending from the first  
21 terminal through the channel to the second terminal.

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25 2. The MOSFET of claim 1 wherein,

26 the gate curvature is defined by a radius extending from a  
27 point inside the first terminal.  
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1 3. The MOSFET of claim 1 wherein,

2 the gate curvature of the gate is defined by a radius  
3 extending from a point inside the first terminal, the gate  
4 curvature is less than a semicircle.

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8 4. The MOSFET of claim 1 wherein,

9 the gate curvature is defined by a radius extending from a  
10 point inside the first terminal, the gate curvature is a  
11 quarter circle.

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15 5. The MOSFET of claim 1 wherein,

16 the gate curvature is defined by a radius extending from a  
17 point inside the first terminal, the gate curvature is an  
18 eighth circle.

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1 6. A MOSFET for receiving an applied voltage and a gate  
2 voltage, the MOSFET comprising,  
3 a source terminal in n-type silicon,  
4 a gate terminal receiving the gate voltage, the gate being  
5 disposed over a channel of the n-type silicon, the gate being  
6 insulated from the n-type silicon, the channel having two  
7 channel ends, the two channel ends being nonparallel nonaligned  
8 channel ends, the curve of the gate and the channel are  
9 noninflecting,  
10 an insulator disposed between the gate and the n-type  
11 silicon, and  
12 a drain terminal in the n-type silicon, the applied voltage  
13 extends between the source terminal and the drain terminal, the  
14 gate voltage serving to control conduction between the source  
15 terminal and the drain terminal in the presence of the gate  
16 voltage, the applied voltage serving to establish a diverging  
17 electric field extending from the source terminal through the  
18 channel to the drain terminal.

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20 7. The MOSFET of claim 6 further comprising,  
21 a silicon substrate,  
22 a p-type well disposed within the substrate, the source  
23 terminal and drain terminal and channel being disposed in the  
24 p-type well.

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26 8. The MOSFET of claim 6 wherein,  
27 th curve of the gate is defined by a radius extending from  
28 a point inside the source terminal.

1 9. The MOSFET of claim 6 wher in,  
2 the gate curvature is defined by a radius extending from a  
3 point inside the source terminal, the gate curvature is less  
4 than a semicircle.

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6 10. The MOSFET of claim 6 wherein,  
7 the gate curvature is defined by a radius extending from a  
8 point inside the source terminal, the gate curvature is a  
9 quarter circle.

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13 11. The MOSFET of claim 6 further comprising,  
14 a p-type silicon well.

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18 12. The MOSFET of claim 6 further comprising,  
19 a source connector,  
20 a source contact in the source connector for connecting the  
21 source connector to the source terminal,  
22 a drain connector, and  
23 a drain contact in the drain connector for connecting the  
24 drain connector to the drain terminal, the applied voltage  
25 being applied between the source connector and the drain  
26 connector.

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1 13. The MOSFET of claim 6 further comprising,  
2 a source connector,  
3 a source contact in the source connector for connecting the  
4 source connector to the source terminal,  
5 a drain connector, and  
6 a plurality of drain contacts in the drain connector for  
7 connecting the drain connector to the drain terminal, the  
8 applied voltage being applied between the source connector and  
9 the drain connector.

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15 14. The MOSFET of claim 6 further comprising,  
16 a p-type silicon well,  
17 a source connector,  
18 a source contact in the source connector for connecting the  
19 source connector to the source terminal,  
20 a drain connector, and  
21 a drain contact in the drain connector for connecting the  
22 drain connector to the drain terminal, the applied voltage  
23 being applied between the source connector and the drain  
24 connector.

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1 15. The MOSFET of claim 6 further comprising,  
2 a p-type silicon well,  
3 a source connector,  
4 a sourc contact in the source connector for connecting the  
5 source connector to the source terminal,  
6 a drain connector, and  
7 a plurality of drain contacts in the drain connector for  
8 connecting the drain connector to the drain terminal, the  
9 applied voltage being applied between the source connector and  
10 the drain connector.

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